REMARKS

Claims 1-3, 5-13 and 15-21 are pending in this application. By this Amendment, claim 21 is amended. Reconsideration of the application is respectfully solicited.

Applicants gratefully acknowledge the courtesies extended to Applicants' representative during the telephone interview conducted August 31, 2004. The substance of the interview is incorporated into the following remarks, which constitute Applicants' record of the interview.

The Office Action objects to claim 21 for informalities. By this Amendment, claim 21 is amended, thereby obviating this grounds of objection. Applicants respectfully request that the objection to claim 21 be withdrawn.

The Office Action rejects claims 1-3, 5-13 and 15-21 under 35 U.S.C. §103(a) over U.S. Patent No. 5,301,325 to Benson in view of U.S. Patent No. 6,035,120 to Ravichandran. This rejection is respectfully traversed.

The Office Action admits that Benson does not explicitly teach that the controller dividing the source code into code blocks based on a target processor register capability, and relies on Ravichandran to supply the missing subject matter. However, Applicants submit that Ravichandran also does not disclose "the controller dividing the source code into code blocks based on a target processor register capability," as recited in claim 1, and similarly recited in claim 11.

Ravichandran discloses: "Step 405 is used to keep track of the available registers in the target processor. This typically means that the register in the target executable is available and is of the correct type ... The actual register renaming is usually implemented using a table indicating whether a particular register is in use or available for use. For example, generally a floating point register used in the source executable is matched to a floating point register in the target executable." (See column 6, lines 4-22).

However, nowhere in Ravichandran is the number of available registers used to divide the source code into code blocks. According to Ravichandran, the source instructions are converted line by line to target processor instructions, based on a conversion table. See, for example, column 5, lines 63-66, which state that "in one embodiment, this step looks up the arithmetic source instruction in the conversion table and maps each instruction associated with the source processor to one or more valid instructions associated with the target processor." Nowhere does Ravichandran teach "the controller dividing the source code into code blocks based on a target processor register capability, wherein the controller identifies source register types as data registers or address registers of the source processor and corresponding target registers of the target processor that correspond to each of the source register types, the controller selecting one or more selected source register types and one or more maximum numbers of corresponding target registers that correspond to the selected source register types as the target register capability," as recited in claim 1 and similarly recited in claim 11.

During the interview, the Examiner asserted that the existence of instructions indicated that the source code had necessarily been divided. However, Applicants submit that the term "instruction" usually refers to a single line of code, not to a code block. Furthermore, there is no disclosure in Ravichandran that the formation of instructions is "based on the target processor register capability."

Accordingly, the combination of Benson and Ravichandran does not disclose, teach or suggest each and every feature of claims 1 and 11. Claims 2, 3, 13 and 15-20 various depend from claims 1 and 11, and are therefore patentable for at least the reasons set forth above with respect to claims 1 and 11, as well as for the additional features they recite.

Ravichandran discloses only a target processor having data registers, such as floating point registers, not data registers and address registers, as recited in claim 21. Accordingly,

Applicants respectfully request that the rejection of claims 1-3, 5-13 and 15-21 under 35 U.S.C. §103(a) be withdrawn.

In view of the foregoing, it is respectfully submitted that this application is in condition for allowance. Favorable reconsideration and prompt allowance of claims 1-3, 5-13 and 15-21 are earnestly solicited.

Should the Examiner believe that anything further would be desirable in order to place this application in even better condition for allowance, the Examiner is invited to contact the undersigned at the telephone number set forth below.

Respectfully submitted,

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